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09/750,198	12/27/2000	Anil Vasudevan	042390.P9018	7014

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EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/750,198	VASUDEVAN, ANIL	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 6-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Papa et al. (US Patent 6,324,608) in view of Eide et al. (US Patent 6,529,978)

As per claim 6, Papa discloses a system comprising:

- A housing; and (fig.1, 101)
- A mainboard disposed within the housing to which memory and a first processor are connected, said mainboard providing a first network interface operatively coupled to the first processor having a first network port and a first network address; (col.4, line 66-col.5, line 10)
- A first peripheral disposed within the housing; (col.5, lines 22-col.6, line 65)
- A second network interface operatively coupled to the mainboard, providing a second network port and a second network address, the second network interface linked in communication with the first peripheral device; and (col.4, line 66-col.6, line 65)
- A communications link between the first and second network interfaces substantially disposed within the housing. (col.4, line 66-col.6, line 65)

Papa discloses all the limitations as above except using packetized messages based on a network transmission protocol to provide communication between the first processor and the first peripheral device. However, Eide discloses any number of hardware devices coupled to I/O interface 16, an interface to a network 22 t provide communications capability using any number of network protocols (e.g IPX, TCP/IP, SNA, etc.), wherein TCP/IP implies packetized messages. (col.5, lines 10-25), (col.8, lines 1-50)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Eide's teaching into Papa's system so as to have a significant need exists in the art for a manner of changing the bindings between IOA's and IOP's in a hierarchical I/O interface with minimal impact on system availability. (col.2, lines 36-40)

As per claim 7, Papa discloses wherein the first network interface and the communications link comprise an Ethernet subnet. (col.2, lines 5-24), (col.3, lines 2-10)

As per claim 8, Papa discloses wherein the communication link comprises a network signal bus built into the mainboard. (col.5, lines 22-35)

As per claim 9, Papa discloses wherein the communications link comprises a token ring. (col.2, lines 5-24)

As per claim 10, Papa discloses wherein the second network interface is built into the first peripheral device; (col.3,lines 1-10), wherein interface inherently built-in into peripheral device to provide communication)

As per claim 11, Papa discloses wherein the second network interface is built into the mainboard. (col.3, lines 1-10)

As per claims 12, 26-27, Papa discloses wherein the peripheral device comprises one of a video subsystem, a memory subsystem, a disk controller and a modem. (col. 4, lines 1-7)

As per claim 13, Papa discloses wherein the mainboard further includes a second processor connected to a third network interface having a third network address and network port connected to the communication link. (col.4, line 66-col.6, line 65)

As per claims 14, 15, 17, Papa discloses a method for enabling communication between a peripheral device disposed within a computing machine having a processor and an application running on the processor, comprising:

- providing a network interface for each of the processor and the peripheral device; (col.4, line 66-col.6, line 65)
- providing a communication link between the network interfaces of the processor and the peripheral device;(col.3, lines 1-10), (col.4, line 66-col.6, line 65)
- creating a network software socket for each of the processor and the peripheral device; (col.4, line 66-col.6, line 65)
- stabling a connection between the processor and the peripheral device; and (col.4, line 66-col.6, line 65)
- generating messages with the application; (col.1, line 64-col.23)

- transferring the messages between the processor and peripheral device using a network transmission protocol. (col.1, line 64-col.23)

Papa discloses all the limitations as above except using packetized messages based on a network transmission protocol. However, Eide discloses any number of hardware devices coupled to I/O interface 16, an interface to a network 22 t provide communications capability using any number of network protocols (e.g IPX, TCP/IP, SNA, etc.), wherein TCP/IP inherently implies packetized messages. (col.5, lines 10-25) , (col.8, lines 1-50)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Eide's teaching into Papa's system so as to have a significant need exists in the art for a manner of changing the bindings between IOA's and IOP's in a hierarchical I/O interface with minimal impact on system availability. (col.2, lines 36-40)

As per claim 16, Papa discloses the method further comprising applying security measures to determine if an application may connect to a particular peripheral device. (col.1, lines 64-67)

As per claim 18, Papa discloses wherein the communications link and the network interfaces comprise an internal Ethernet network. (col.2, lines 5-24)

As per claim 19, Papa discloses wherein the communications link and the network interfaces comprises an internal token ring network. (col.2, lines 5-24)

As per claim 20, Papa discloses the system further comprising:

A storage device on which software is stored, the software comprising machine instructions that are executable by the first processor that includes a socket application interface (API) that binds the address of the first peripheral device to the second network port and a network interface abstraction layer that provides an abstracted interface that enables an application to communicate with the first peripheral device using a networking protocol. (col.3, lines 1-10), (col.3, line 53-col.4, line55)

As per claim 21, Papa discloses an apparatus, comprising:

- A housing;(fig.1, 101)
- A first processor disposed within the housing;(col.3, line 61-col.4, line 37)
- A first network interface coupled to the first processor, the first network interface having a first network address; (col.4, line 66-col.5, line 10, wherein multiple slots for multiple device implies different address for different interface)
- A peripheral device disposed within the housing; (col.4, line 66-col.5, line 10)
- A second network interface coupled to the peripheral device and having a second network address; and (col.4, line 66-col.5, line 10)
- A network communication link disposed within the housing and (col.4, line 66-col.5, line 35)

Papa discloses all the limitations as above except using packetized messages based on a network transmission protocol to provide

communication between the first network interface and the second network interface. However, Eide discloses any number of hardware devices coupled to I/O interface 16, an interface to a network 22 t provide communications capability using any number of network protocols (e.g IPX, TCP/IP, SNA, etc.), wherein TCP/IP implies packetized messages. (col.5, lines 10-25), (col.8, lines 1-50)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Eide's teaching into Papa's system so as to have a significant need exists in the art for a manner of changing the bindings between IOA's and IOP's in a hierarchical I/O interface with minimal impact on system availability. (col.2, lines 36-40)

As per claim 22, Papa discloses wherein a software application executable by the first processor communicates with the peripheral device via a connection over the network communication link associating the first network address with the second network address. (col.4, line 66-col.6, line 65)

As per claim 23, Papa discloses wherein the first network interface includes a first port address in addition to the first network address to create a first software socket for communicating with the processor and wherein the second network interface includes a second port address in addition to the second network address to create a second software socket for communicating with the peripheral device. (col.4, line 66-col.6, line 65)

As per claim 25, Papa discloses wherein the second network interface comprises a build-in network interface included within the peripheral device. (col.4, line 66-col.6, line 65)

As per claim 28, Papa discloses wherein the peripheral device comprises an external network interface to couple to an external network external to the housing. (fig.2, wherein canister a couple canister b via pc bus 214 implies external housing), (col.4, lines 43-55)

As per claim 29, Papa discloses wherein the external network interface includes a network address translation("NAT") device to translate network addresses between the external network and the network communication link. (col.3, lines 1-10)

As per claim 30, Papa discloses the apparatus further comprising:

- A second processor disposed within the housing; and (col.4, line 66-col.5, line 10)
- A third network interface coupled to the second processor and to the network communication link, the third network interface having a third network address to communicate with the peripheral device via the network communication link. (col.4, line 66-col.6, line 65)

Response to Amendment

3. Applicant's amendment filed on 2/25/05 have been fully considered but not place an application in condition for allowance.

a. Applicant argues that Eide discloses a software for coordinating low level communications within I/O interface 16 does not imply use of packets. There is no centralized software entity coordinating communications between the entieies coupled to the network. A computer using a system bus having a data bus and an address bus, a bus manager does coordinates access to the system bus, packets simply have no meaning to a system bus. Thus, I/O interface 16 communicates with external network 22 using packets, but Eide does not disclose I/O interface 16 or IOPs 44 communicating with processor 12 using packets, as the claim recite. Examiner respectfully disagrees. As Eide notes at col.6, lines 28-65, discloses binding IOA and/or IOP (44 and/or 46) to computer system without having to physically move by incorporating a plurality of software components that implement the dynamic binding capability of I/O interface 16, ie user inputs supplied through user interface through direct software control provided by another software component. A bus manager component handles control of a system I/O bus which coordinates the low level communications within I/O interface 16. Outside of the additional logic incorporated to implement dynamic binding. As previously office action, Examiner already explained that external communication(peripheral devices) with apparatus 10(system) is handled through an input/output (I/O interface 16) coupled and implemented by the processing complex 11(included processor 12) and the communication between the external devices and systems is handled through

interface16 and processor 12 via transmitting/receiving commands on the system (the commands implementations/configurations by softwares wrapped up with packet as a whole to transmit from one device to another which included data a header containing an identification number source and destination addresses) so this implies packetized which is equivalent to applicant's claimed as using packetized. Thus, the prior art teaches the invention as claimed and the claims do not distinguish over the prior art as applied.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. If attempts to*

reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached at (571)272-3632 or via e-mail addressed to [mark.Rinehart@uspto.gov].

The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Kim Huynh

May 3, 2005

TIM VO
PRIMARY EXAMINER